Claims

[c1] 1. A polysilicon thin film transistor, comprising:

a poly-island layer;

a gate over the poly-island layer;

a gate insulation layer between the gate and the poly-island layer; and

an inter-layer dielectric layer, wherein the inter-layer dielectric layer includes an oxide layer and a nitride layer, the oxide layer covers the gate and the gate insulation layer and the nitride layer is over the oxide layer, the oxide layer and the nitride layer of the inter-layer dielectric layer have a thickness relationship given by the following inequality: $T_{ox} \geq (T_{nitride} \times 9000\text{Å})^{1/2}$, where T_{ox} represents the thickness of the oxide layer (in Å), $T_{nitride}$ represents thickness of the silicon nitride layer and that thickness of the nitride layer is between 50Å and 1000Å.

[c2] 2. The polysilicon thin film transistor of claim 1, wherein the poly-island layer further comprises:

a channel region underneath the gate; and

a source/drain region on each side of the channel region.

[c3] 3. The polysilicon thin film transistor of claim 2, wherein

the transistor may further include a lightly doped drain region between the channel region and the source/drain region.

[c4] 4. A method of forming a polysilicon thin film transistor, comprising the steps of:

forming a poly-island layer over a substrate;

forming a gate insulation layer over the poly-island layer;

forming a gate electrode over the gate insulation layer above a section of the poly-island layer destined for forming a channel region;

conducting an ion implantation of the poly-island layer using the gate as a mask to form source/drain regions in the poly-island layer outside the channel region; and

sequentially forming an oxide layer and a nitride layer over the substrate to cover the gate and the gate insulation layer, wherein the oxide layer and the nitride layer of the inter-layer dielectric layer have a thickness relationship given by the following inequality: $T_{ox} \geq (T_{nitride} \times 9000\text{Å})^{1/2}$, where T_{ox} represents the thickness of the oxide layer (in Å), $T_{nitride}$ represents thickness of the silicon nitride layer and that thickness of the nitride layer is between 50Å and 1000Å.

[c5] 5. The method of claim 4, wherein the step of forming the poly-island layer over the substrate includes the

sub-steps of:

depositing amorphous silicon over the substrate;

conducting a laser crystallization or an excimer laser annealing process to melt the amorphous silicon and recrystallize into a polysilicon layer; and

conducting photolithographic and etching processes to form islands of polysilicon.

[c6]   6. The method of claim 4, wherein after forming the poly-island layer over the substrate, further includes conducting a channel ion implantation so that the poly-island layer contains dopants.

[c7]   7. The method of claim 4, wherein the step of forming a gate insulation layer over the poly-island layer includes carrying out a plasma-enhanced chemical vapor deposition.

[c8]   8. The method of claim 4, wherein the method may further include the step of forming a lightly doped drain structure between the source/drain region and the channel region.